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09/878,270	06/12/2001	Kenichi Miki	047912-0136	2988

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

4

Office Action Summary	Application No.	Applicant(s)	
	09/878,270	MIKI, KENICHI	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: '101' and '102' in Figure 3. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The abstract of the disclosure is objected to because the specification contains reference numerals to the drawings (the reference numerals to the drawings should be removed). Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 6 and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites, "each of said divided data items and said parity data are set to have an equal capacity" is incomprehensible since data items and parity data items refer to the data and it is not clear how data can have a capacity. Did the Applicant intend length? Claim 7 depends from claim 6; hence inherits the deficiencies of claim 6

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Flora, Laurence P. et al. (US 4722085 A, hereafter referred to as Flora).

35 U.S.C. 102(b) rejection of claim 1.

Flora teaches a method for controlling a data read/write operation (see Abstract and Figure 2 in Flora; Note: Storage Control Unit 30 and Read/Write Interface 25 in Figure 2 are a controller for controlling a data read/write operation) comprising: a data receiving step of receiving predetermined data to be written to a disk from an upper-level host system (col. 1, lines 8-15 in Flora teach that the storage system of Figure 2 is for use in a data processing system which comprises a host computer and peripheral devices which in the case of the teachings in Flora would include the peripheral storage device of Figure 2); a data processing step of conducting predetermined processing on said

received data (Data Organizer 34 in Figure 3 of Flora is a device for performing a data processing step of conducting predetermined processing on said received data); and a data write-in step of writing said processed data to said disk (Note: the Data Organizer 34 in Figure 3 is a component within the Read/Write Interface 25 in Figure 2 of Flora), wherein said data processing step comprises: a data dividing step of dividing said data received at said data receiving step into a plurality of data items and also generating parity data (col. 3, lines 48-67 of Flora teach that 32 disk sectors are divided into 2048 words, each word comprised of 32 bits, B0-B31, and Error Circuitry 32 in Figure 3 of Flora adds 7 check-bits, i.e., parity, to each word, one word at a time; Note: the matrix array comprising the 2048 words in Figure 4 is divided into 32 columns and 7 check-bits of parity are produced for each word in each row to create an additional 7 columns so that the 2048 words are divided into 32 columns of data, labeled B0-B31, and 7 columns of check-bit parity, corresponding to check-bit parity data items B32-B38; hence each word comprises 32 data items, B0-B31, and 7 check-bit parity data items, B32-B38); a data storing step of individually storing said divided data items and said parity data items into cache modules respectively (each column of data, corresponding to data items B0-B31, and each columns of parity, corresponding to check-bit parity data items B32-B38, is serially stored in respective buffers 13-0 to 13-38); a data repairing step of fetching said divided data items and said parity data from said cache modules and repairing one of said divided data items, if said one is damaged (col. 5, lines 1-25 of Flora teach that data is fetched from the disk array by temporarily storing the respective data items, B0-B31, and check-bit parity data items, B32-B38, in

respective buffers and correcting any single bit of error in each word if an error is detected), using said parity data; and a data combining step of combining said divided data items (col. 5, lines 1-25 of Flora teach that the Data Organizer 34 rearranges the data for transmission to the storage control unit 30).

Note: the IEEE Authoritative Dictionary of IEEE Standard Terms defines a data processing system as a system including computer and associated personal that performs input, processing, storage output, and control functions to accomplish a sequence of operations on data. In addition, the IEEE Authoritative Dictionary of IEEE Standard Terms defines host as a device, typically a computer that will control the communication with attached peripherals. Hence since a data processing system generally comprises a computer for performing processing, storage output, and control functions to accomplish a sequence of operations on data a data processing system inherently comprises a host computer, i.e. a host system, for controlling communication with attached peripherals.

Note: the IEEE Authoritative Dictionary of IEEE Standard Terms defines cache as a buffer inserted between one or more processors and the bus, used to hold currently active copies of blocks from main memory. Since the buffers in Flora are designed to be connected between a computer and main disk array memory for temporary storage, they are cache.

35 U.S.C. 102(b) rejection of claim 2.

Note: MPEP § 2131.01(III) states an extra reference or evidence can be used to show an inherent characteristic of the thing taught by the primary reference: "To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991).

Accordingly, the Examiner introduces the Wicker reference (Stephen B. Wicker, "Error Control Systems for Digital Communication and Storage", Prentice-Hall, 1995, Pages 116-121) as a teaching reference for that which is inherent in the Flora patent. Flora, in column 5, lines 10-25, teaches that the error correction circuitry in the Flora patent operates in a conventional manner. Wicker, on the other hand, teaches the conventional algorithm for decoding systematic codes, i.e., codewords that are comprised of message bits and corresponding check-bit parity data items.

Flora teaches a method for controlling a data read/write operation (see Abstract and Figure 2 in Flora; Note: Storage Control Unit 30 and Read/Write Interface 25 in Figure 2 are a controller for controlling a data read/write operation) comprising: a data read-out step of reading out predetermined data to be transmitted to an upper-level host system from a disk (col. 4, lines 65-68 and col. 5, lines 1-9 in Flora teach a data read-out step of reading out predetermined data to be transmitted to an upper-level host system from a disk in response to the transfer signal Tr); a data processing step of conducting

predetermined processing on said read out data (the read out processing taught in col. 4, lines 65-68 and col. 5, lines 1-25 in Flora is a data processing step of conducting predetermined processing on said read out data); and a data transmitting step of transmitting said processed data to said upper-level host system (col. 5, lines 21-25 in Flora teach a data transmitting step of transmitting said processed data to said upper-level host system), wherein said data processing step comprises: a data dividing step of dividing said data read out at said data read-out step into a plurality of data items (Note: each of the words read out of the disk array are divided by controllers 12-0 to 12-31 in Figure 3 of Flora into data items, B0-B31) and also generating parity data (controllers 12-32 to 12-38 in Figure 3 of Flora generate parity check-bit data by applying a read operation to extract the parity check-bit data from the disk array; Note: Miriam-Webster's dictionary defines generate as to define or originate by the application of one or more rules or operations); a data storing step of individually storing said divided data items and said parity data items into cache modules respectively (in Figure 3 of Flora data items, B0-B31, are stored in respective buffers, 13-0 to 13-31, and check-bit parity data items, B32-B38, are stored in respective buffers, 13-32 to 13-38); a data repairing step of fetching said divided data items and said parity data from said cache modules and also repairing one of said divided data, if said one is damaged, using said parity data (col. 5, lines 1-25 of Flora teach that data is fetched from the disk array by temporarily storing the respective data items, B0-B31, and check-bit parity data items, B32-B38, in respective buffers and correcting any single bit of error in each word if an error is detected); and a data combining step of combining said divided data (col. 5,

lines 1-25 of Flora teach that the Data Organizer 34 rearranges the data for transmission to the storage control unit 30).

Note: the IEEE Authoritative Dictionary of IEEE Standard Terms defines a data processing system as a system including computer and associated personal that performs input, processing, storage output, and control functions to accomplish a sequence of operations on data. In addition, the IEEE Authoritative Dictionary of IEEE Standard Terms defines host as a device, typically a computer that will control the communication with attached peripherals. Hence since a data processing system generally comprises a computer for performing processing, storage output, and control functions to accomplish a sequence of operations on data, a data processing system inherently comprises a host computer, i.e. a host system, for controlling communication with attached peripherals.

Note: the IEEE Authoritative Dictionary of IEEE Standard Terms defines cache as a buffer inserted between one or more processors and the bus, used to hold currently active copies of blocks from main memory. Since the buffers in Flora are designed to be connected between a computer and main disk array memory for temporary storage, they are cache.

35 U.S.C. 102(b) rejection of claim 3.

Flora teaches a disk array apparatus (Figure 3 in flora is an exemplary disk array apparatus) comprising an array controlling unit for receiving an instruction from an upper-level host system to thereby write predetermined data to or read said

predetermined data out from a disk and also conduct operational processing on said predetermined data (Read/Write Interface 25 in Figure 2 and 3 of Flora is an array controlling unit for receiving an instruction from an upper-level host system to thereby write predetermined data to or read said predetermined data out from a disk and also conduct operational processing on said predetermined data; Note: the read/write processing taught in col. 3, lines 48-68, col. 4, lines 1-23, col. 4, lines 65-68 and col. 5, lines 1-25 in Flora are read/write data processing steps for conducting predetermined processing on read/write data), wherein said array controlling unit comprises: a data dividing function for dividing said predetermined data into at least two data items (Data Organizer 34 in Flora is a data dividing function for dividing said predetermined data into at least two data items) and also generating parity data for said predetermined data (Error Circuitry 34 in Flora is a means for generating parity data for said predetermined data); and a data combining function for repairing one of said divided data items, if said one is damaged, using said parity data (during read out Read/Write Interface 25 in Figure 2 and 3 of Flora perform a data combining function for repairing one of said divided data items using Error Circuitry 34 in Flora, if said one is damaged, using said parity data) and also combining said divided data items (Data Organizer 34 in Flora is a means for combining said divided data items).

Note: the IEEE Authoritative Dictionary of IEEE Standard Terms defines a data processing system as a system including computer and associated personal that performs input, processing, storage output, and control functions to accomplish a sequence of operations on data. In addition, the IEEE Authoritative Dictionary of IEEE

Standard Terms defines host as a device, typically a computer that will control the communication with attached peripherals. Hence since a data processing system generally comprises a computer for performing processing, storage output, and control functions to accomplish a sequence of operations on data a data processing system inherently comprises a host computer, i.e. a host system, for controlling communication with attached peripherals.

Note: the IEEE Authoritative Dictionary of IEEE Standard Terms defines cache as a buffer inserted between one or more processors and the bus, used to hold currently active copies of blocks from main memory. Since the buffers in Flora are designed to be connected between a computer and main disk array memory for temporary storage, they are cache.

35 U.S.C. 102(b) rejection of claim 4.

Flora teaches a disk array apparatus (Figure 3 in flora is an exemplary disk array apparatus) comprising an array controlling unit for receiving an instruction from an upper-level host system to thereby write predetermined data to or reading said predetermined data from a disk and also conduct operational processing on said predetermined data (Read/Write Interface 25 in Figure 2 and 3 of Flora is an array controlling unit for receiving an instruction from an upper-level host system to thereby write predetermined data to or read said predetermined data out from a disk and also conduct operational processing on said predetermined data; Note: the read/write processing taught in col. 3, lines 48-68, col. 4, lines 1-23, col. 4, lines 65-68 and col. 5,

lines 1-25 in Flora are read/write data processing steps for conducting predetermined processing on read/write data), wherein said array controlling unit comprises: a data dividing section for dividing said predetermined data into at least two data items (Data Organizer 34 in Flora is a data dividing function for dividing said predetermined data into at least two data items) and also generating parity data for said predetermined data (Error Circuitry 34 in Flora is a means for generating parity data for said predetermined data); a plurality of cache modules for temporarily storing said divided data items and said parity data respectively (Buffers 13-0 to 13-38 are a plurality of cache modules for temporarily storing said divided data items and said parity data respectively); and a data combining section for repairing said divided data item stored in one of said cache modules, if said one fails, using the remaining ones of said divided data items and said parity data (during read out Read/Write Interface 25 in Figure 2 and 3 of Flora perform a data combining function for repairing one of said divided data items using Error Circuitry 34 in Flora, if said one is damaged, using said parity data) and also combining said divided data items (Data Organizer 34 in Flora is a means for combining said divided data items).

Note: the IEEE Authoritative Dictionary of IEEE Standard Terms defines a data processing system as a system including computer and associated personal that performs input, processing, storage output, and control functions to accomplish a sequence of operations on data. In addition, the IEEE Authoritative Dictionary of IEEE Standard Terms defines host as a device, typically a computer that will control the communication with attached peripherals. Hence since a data processing system

generally comprises a computer for performing processing, storage output, and control functions to accomplish a sequence of operations on data a data processing system inherently comprises a host computer, i.e. a host system, for controlling communication with attached peripherals.

Note: the IEEE Authoritative Dictionary of IEEE Standard Terms defines cache as a buffer inserted between one or more processors and the bus, used to hold currently active copies of blocks from main memory. Since the buffers in Flora are designed to be connected between a computer and main disk array memory for temporary storage, they are cache.

35 U.S.C. 102(b) rejection of claims 5 and 6.

Each of the Buffers 13-0 to 13-38 in Figure 3 of Flora stores 2048 bit, one bit respectively from each of 2048 words, hence has equal capacity.

35 U.S.C. 102(b) rejection of claim 7.

Col. 3, lines 48-67 of Flora teach that 32 disk sectors are divided into 2048 words, each word comprised of 32 bits, B0-B31, and Error Circuitry 32 in Figure 3 of Flora adds 7 check-bits, i.e., parity, to each word, one word at a time; Note: the matrix array comprising the 2048 words in Figure 4 is divided into 32 columns and 7 check-bits of parity are produced for each word in each row to create an additional 7 columns so that the 2048 words are divided into 32 columns of data, labeled B0-B31, and 7 columns of check-bit parity, corresponding to check-bit parity data items B32-B38; hence each word

comprises 32 data items, B0-B31, and 7 check-bit parity data items, B32-B38, and each column of data, corresponding to data items B0-B31, and each columns of parity, corresponding to check-bit parity data items B32-B38, is serially stored in respective buffers 13-0 to 13-38.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Flora, Laurence P. et al. (US 4722085 A, hereafter referred to as Flora).

35 U.S.C. 103(a) rejection of claim 8.

Flora, substantially teaches the claimed invention described in claims 1-7 (as rejected above).

However Flora, does not explicitly teach the specific use of the number of said divided data items is set one smaller than a number of a number of said cache modules.

The Examiner asserts that it would have been an obvious Engineering Design choice based on availability of components, choice of error correction codes and circuit requirements to combine buffers so that the number of said divided data items is set one smaller than a number of a number of said cache modules. For example, if an error correction code generating 8-bit parity was used, then 4 data modules could be used for B0-B7, B8-B15, B16-B23 and B24-B31 and a 5^{th} module could be used for the check-bit parity data items B32-B39. One of ordinary skill in the art at the time the invention was made would have been highly motivated to make such changes based on the design requirements for circuitry and error correction capabilities.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Flora by including use of the number of said divided data items set to one smaller than the number of a number of said cache modules. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of the number of said divided data items set to one smaller than the number of a number of said cache modules would have provided the opportunity to make changes to the preferred embodiment taught in the Flora patent based on the design requirements for circuitry and error correction capabilities to provide an alternative embodiment of the teachings in the Flora patent based on obvious engineering design choices given a set of particular design requirements without

deviating from the scope or intent of the teachings in the Flora patent (col. 6, lines 1-5. Flora).

35 U.S.C. 103(a) rejection of claim 9.

Flora teaches a disk array apparatus (Figure 3 in flora is an exemplary disk array apparatus) comprising an array controlling unit for receiving an instruction from an upper-level host system to thereby write predetermined data to or reading said predetermined data from a disk and also conduct operational processing on said predetermined data (Read/Write Interface 25 in Figure 2 and 3 of Flora is an array controlling unit for receiving an instruction from an upper-level host system to thereby write predetermined data to or read said predetermined data out from a disk and also conduct operational processing on said predetermined data; Note: the read/write processing taught in col. 3, lines 48-68, col. 4, lines 1-23, col. 4, lines 65-68 and col. 5, lines 1-25 in Flora are read/write data processing steps for conducting predetermined processing on read/write data), wherein said array controlling unit comprises: a data dividing section for dividing said predetermined data into at least two data items (Data Organizer 34 in Flora is a data dividing function for dividing said predetermined data into at least two data items) and also generating parity data for said predetermined data (Error Circuitry 34 in Flora is a means for generating parity data for said predetermined data); a plurality of cache modules for temporarily storing said divided data items and said parity data respectively (Buffers 13-0 to 13-38 are a plurality of cache modules for temporarily storing said divided data items and said parity data respectively); and a data

combining section for repairing said divided data item stored in one of said cache modules, if said one fails, using the remaining ones of said divided data items and said parity data (during read out Read/Write Interface 25 in Figure 2 and 3 of Flora perform a data combining function for repairing one of said divided data items using Error Circuitry 34 in Flora, if said one is damaged, using said parity data) and also combining said divided data items (Data Organizer 34 in Flora is a means for combining said divided data items).

Note: the IEEE Authoritative Dictionary of IEEE Standard Terms defines a data processing system as a system including computer and associated personal that performs input, processing, storage output, and control functions to accomplish a sequence of operations on data. In addition, the IEEE Authoritative Dictionary of IEEE Standard Terms defines host as a device, typically a computer that will control the communication with attached peripherals. Hence since a data processing system generally comprises a computer for performing processing, storage output, and control functions to accomplish a sequence of operations on data a data processing system inherently comprises a host computer, i.e. a host system, for controlling communication with attached peripherals.

Note: the IEEE Authoritative Dictionary of IEEE Standard Terms defines cache as a buffer inserted between one or more processors and the bus, used to hold currently active copies of blocks from main memory. Since the buffers in Flora are designed to be connected between a computer and main disk array memory for temporary storage, they are cache.

However Flora, does not explicitly teach the specific use of a recording medium for recording a data read/write controlling program.

The Examiner asserts that it would be obvious to use a software control program in place of a hardware control program based on obvious Engineering design choice such as available circuit space, available storage for software and requirements associated with capability to be upgraded. One of ordinary skill in the art at the time the invention was made would have been highly motivated to make such changes based on the design requirements for the storage system.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Flora by including use of a recording medium for recording a data read/write-controlling program. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a recording medium for recording a data read/write controlling program would have provided the opportunity to implement the preferred embodiment of the storage system taught in the Flora patent in a data processing environment based on design requirements for the data processing system by providing a required mechanism in the Flora patent for controlling read/write operations based on obvious engineering design choices given a set of particular design requirements without deviating from the scope or intent of the teachings in the Flora patent (col. 6, lines 1-5. Flora).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yashiro, Mitsuhiko et al. (US 5787460 A) teaches a disk array apparatus for forming redundant information when updating data stored in a disk apparatus. Arai, Kouji et al. (US 5564116 A) teaches an array type storage unit system in which an increase in the storage units (for the purpose of improving data transfer speed), an increase of a storage capacity or an increase of redundancy is performed dynamically without stop of the system. Franaszek, Peter A. et al. (US 5522032 A) teaches disk array systems which create and store parity blocks in order to facilitate recovery from a disk failure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph D. Torres, PhD
Art Unit 2133